ALPHA DATA

FMC-RCP-10G
User Manual

Revision: V1.0

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1 Introduction

The FMC-RCP-10G ("the FMC") is a front panel adapter card with up to four 10Gb/s Optical transceiver channels.

The FMC is electrically compliant with VITA 57.1 FMC standard but has a modified profile and increased front IO area to accommodate the optical transceivers.

The FMC is electrically and physically compatible with the Alpha Data ADM-VPX3-7V2. Please contact Alpha Data for details of compatibility with other FMC carriers.

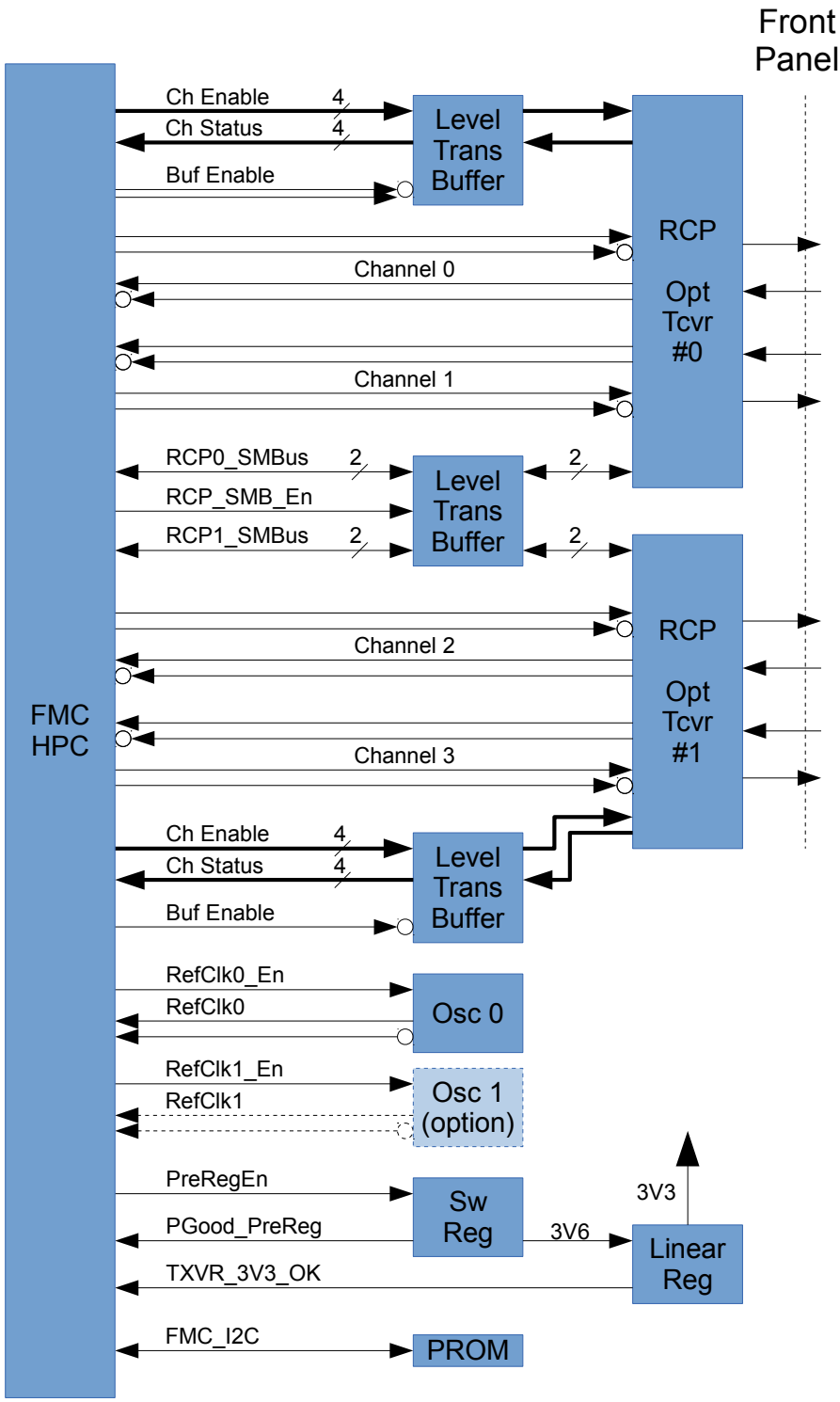

Figure 1 : FMC-RCP-10G

2 Installation

The XRM-RCP-10G is designed to plug in to the FMC front panel connector on a compatible carrier. The retaining screws should be tightened to secure the FMC.

Note: This operation should not be performed while the host/carrier card is powered up.

2.1 Handling instructions

2.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

2.2 IO Voltage Selection

The FMC IO voltage is adjustable within a range specified in I2C ROM. The carrier is responsible for reading the contents of the ROM and setting VADJ to the correct level.

The VADJ "required value" in the ROM is 1.8V but the "min" and "max" values are 1.65V and 3.4V respectively. The FMC-RCP-10G may operate with VADJ at any voltage within this range.

3 Specification

3.1 Optical Transceiver Module

The FMC is fitted with one or two COTSWORKS "RCP" Optical transceiver modules, type RCP-10G-SX-DX-LX-R-A. Each RCP module has four independent optical channels (two Transmit and two Receive).

Tx Channels	2 (lanes 0 and 3)
Rx Channels	2 (lanes 1 and 2)
Data Rate	1.0 to 10.3125Gb/s
Optical Wavelength	850nm
Front Connector	ARINC 801 1.25mm LuxCis
Operating Temp	-40°C to +85°C
Storage Temp	-55°C to +100°C

Table 1 : RCP Module Specification

3.2 Cabling

Compatible Multi-mode fibre cables are available directly from COTSWORKS and other vendors

3.2.1 Cable Tools

Spcialist tools are required to insert and remove the LuxCis connectors from the optical module.

The AICONICS USA "all in one" tool (p/n M81969/1-03) is a low-cost option that is suitable for insertion and removal. Other types are available from different vendors.

3.3 Clocks

The FMC is fitted with one 156.250MHz LVDS Oscillator as standard. This provides a reference clock to the carrier on GBTCLK0_M2C. A different frequency may be specified as an ordering option.

The FMC can accommodate a second LVDS oscillator to provide a second reference to the carrier on GBTCLK1. This is not fitted as standard, but may be specified as an ordering option. Please contact Alpha Data for details.

4 Ordering Information

FMC-RCP-10G/l(f0)(c)(a)		
Lanes	l	2 = 2 Tx + 2 Rx lanes (one RCP module) 4 = 4 Tx + 4 Rx lanes (two RCP modules)
Ref0 Frequency	f0	blank = 156.250MHz /xxx.yyy (specify frequency in MHz)
Cooling	c	blank = air-cooled industrial, /CC1 = conduction-cooled industrial
Conformal Coating	a	blank = no coating, A = Acrylic (Humiseal 1B31), P = Polyurethane (Arathane 5750)

Table 2 : Ordering Information

5 Related Documents

ANSI/VITA 57.1, FPGA Mezzanine Card (FMC) Standard, 2010, ISBN 1-885731-49-3

6 FMC Pinout

Signal	Dir	Description	FMC Name	FMC Pin
Tx0_P	I	Link 0 Tx (True)	DP_C2M_P0	C2
Tx0_N	I	Link 0 Tx (Comp)	DP_C2M_N0	C3
Tx1_P	I	Link 1 Tx (True)	DP_C2M_P1	A22
Tx1_N	I	Link 1 Tx (Comp)	DP_C2M_N1	A23
Tx2_P	I	Link 2 Tx (True)	DP_C2M_P2	A26
Tx2_N	I	Link 2 Tx (Comp)	DP_C2M_N2	A27
Tx3_P	I	Link 3 Tx (True)	DP_C2M_P3	A30
Tx3_N	I	Link 3 Tx (Comp)	DP_C2M_N3	A31
Rx0_P	O	Link 0 Rx (True)	DP_M2C_P0	C6
Rx0_N	O	Link 0 Rx (Comp)	DP_M2C_N0	C7
Rx1_P	O	Link 1 Rx (True)	DP_M2C_P1	A2
Rx1_N	O	Link 1 Rx (Comp)	DP_M2C_N1	A3
Rx2_P	O	Link 2 Rx (True)	DP_M2C_P2	A6
Rx2_N	O	Link 2 Rx (Comp)	DP_M2C_N2	A7
Rx3_P	O	Link 3 Rx (True)	DP_M2C_P3	A10
Rx3_N	O	Link 3 Rx (Comp)	DP_M2C_N3	A11

Table 3 : HSSIO Links

Signal	Dir	Description	FMC Name	FMC Pin
TXCHEN0_N	I	Tx Ch 0 Enable (Active Low)	LA05_P	D11
TXCHEN1_N	I	Tx Ch 1 Enable (Active Low)	LA05_N	D12
TXCHEN2_N	I	Tx Ch 2 Enable (Active Low)	LA09_P	D14
TXCHEN3_N	I	Tx Ch 3 Enable (Active Low)	LA09_N	D15
RXCHEN0_N	I	Rx Ch 0 Enable (Active Low)	LA04_P	H10
RXCHEN1_N	I	Rx Ch 1 Enable (Active Low)	LA04_N	H11
RXCHEN2_N	I	Rx Ch 2 Enable (Active Low)	LA08_P	G12
RXCHEN3_N	I	Rx Ch 3 Enable (Active Low)	LA08_N	G13
TXFLT0	O	Tx Channel 0 Fault	LA07_P	H13
TXFLT1	O	Tx Channel 1 Fault	LA07_N	H14
TXFLT2	O	Tx Channel 2 Fault	LA11_P	H16
TXFLT3	O	Tx Channel 3 Fault	LA11_N	H17
RXLOS0	O	Rx Channel 0 Loss-Of-Sync	LA06_P	C10
RXLOS1	O	Rx Channel 1 Loss-Of-Sync	LA06_N	C11

Table 4 : Link Control (continued on next page)

Signal	Dir	Description	FMC Name	FMC Pin
RXLOS2	O	Rx Channel 2 Loss-Of-Sync	LA10_P	C14
RXLOS3	O	Rx Channel 3 Loss-Of-Sync	LA10_N	C15

Table 4 : Link Control

Signal	Dir	Description	FMC Name	FMC Pin
RefClk0_EN	I	Ref Clock 0 Enable	LA13_P	D17
RefClk1_EN	I	Ref Clock 1 Enable	LA13_N	D18
RefClk0_P	O	Ref Clock 0 (True)	GBTCLK0_M2C_P	D4
RefClk0_N	O	Ref Clock 0 (Comp)	GBTCLK0_M2C_N	D5
RefClk1_P	O	Ref Clock 1 (True)	GBTCLK1_M2C_P	B20
RefClk1_N	O	Ref Clock 1 (Comp)	GBTCLK1_M2C_N	B21

Table 5 : Clocks

Signal	Dir	Description	FMC Name	FMC Pin
FMC_SCL	I	IPMI Clock	SCL	C30
FMC_SDA	IO	IPMI Data	SDA	C31
FMC_GA0	I	IPMI Geo Address(0)	GA0	C34
FMC_GA1	I	IPMI Geo Address(1)	GA0	D35
RCP_SMB_EN	I	Enable RCP Module SMB	LA02_P	H7
RCP0_SCLK	I	RCP Module 0 SMB Clock	LA00_N_CC	G7
RCP0_SDA	IO	RCP Module 0 SMB Data	LA00_P_CC	G6
RCP0_INT	O	RCP Module 0 SMB Irpt	LA14_P	C18
RCP1_SCLK	I	RCP Module 1 SMB Clock	LA01_N_CC	D9
RCP1_SDA	IO	RCP Module 1 SMB Data	LA01_P_CC	D8
RCP1_INT	O	RCP Module 1 SMB Irpt	LA14_N	C19

Table 6 : I2C

Signal	Dir	Description	FMC Name	FMC Pin
PreRegEn	I	Enable RCP Power Pre-Regulator	LA16_P	G18
RCP0En_L	I	Enable RCP Module 0 (Active Low)	LA03_P	G9
RCP1En_L	I	Enable RCP Module 1 (Active Low)	LA03_N	G10
PGOOD_PREREG	O	RCP Power Pre-Regulator Status	LA15_P	H19
TXVR_3V3_OK	O	RCP 3V3 Regulator Status	LA15_N	H20

Table 7 : Power Supply Control

7 Board Layout

Revision History

Date	Revision	Nature of Change
14/4/14	0.1	First Draft
9/6/14	1.0	Figure 1: Additional detail to diagram,Table 4: Corrected polarity of Tx and Rx enables, minor corrections.

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